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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/872,796	06/01/2001	Craig L. Stevens	10001.000600 (NVLS 379)	4156

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EXAMINER	
KIELIN, ERIK J	
ART UNIT	**PAPER NUMBER**
2813	

DATE MAILED: 03/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/872,796	Applicant(s) STEVENS ET AL.	
	Examiner Erik Kielin	Art Unit 2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9-13,17 and 19-21* is/are pending in the application.

4a) Of the above claim(s) *none* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-13,17 and 19-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This action responds to the Amendment filed 18 December 2003.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims **1**-7, 9-13, and **17**, 19-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Independent claims 1 and 17 recite the limitation, "the robot being exposed to atmosphere." The metes and bounds of "atmosphere" are considered unclear because the atmosphere is undefined. If Applicant means the atmosphere surrounding the earth, then the claim is not enabled because the "atmospheric robot 201" disclosed in the specification and the drawings is clearly shown to be in a chamber which isolated from "the atmosphere." Alternatively, the atmosphere may be any atmosphere surrounding the robot within the chamber in which it resides.

For the purposes of patentability, the claims will be interpreted as best understood, with the broadest reasonable interpretation of the word "atmosphere."

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-7, 9-13 and **17**, 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,251,759 B1 (**Guo** et al.) in view of US 6,270,582 B1 (**Rivkin** et al.).

Regarding independent claims 1 and 17, **Guo** discloses a wafer processing system comprising:

a load lock **114** (Fig. 1);

a transport module having a load chamber **113** (called "buffer chamber" in Guo), a transfer chamber **101**, and a pass-through chamber **122** (additionally called "transition chambers" in Guo col. 4, line 19) located between the load chamber **113** and the transfer chamber **101**, the load chamber being coupled to the load lock **114**;

an intermediate process module **124** (called "transition chambers" in Guo col. 4, line 19) coupled to the load chamber and the transfer chamber (as further limited by instant claim 20);

a loader **130** configured to receive a plurality of wafers to be processed;

a robot **119** configured to transfer a wafer between the load lock **114** and the loader **130**, the robot **119** being exposed to atmosphere;

a first set of process modules **116, 118, 121** coupled to the load chamber **113**;

a second set of process modules **104, 106, 108, 110** coupled to the transfer chamber.

Note that the word "atmosphere" is taken to be that atmosphere within the buffer chamber.

Guo does not indicate if the load lock has "only one pedestal configured to support a single wafer thereon **during a pump down of the load lock**," as presently amended. (Emphasis

added.) Further regarding claim 1 and claim 19, **Guo** does not teach that the pedestal has an integral cooling unit (instant claim 1) which is water-cooled (instant claim 19).

Rivkin teaches a single-wafer load lock (title) for a multi-chamber semiconductor wafer process module having a water-cooled, single-wafer pedestal **136, 182, 184** (Fig. 3; col. 6, lines 1-4, lines 37-47). **Rivkin** teaches that only one pedestal **182** (called wafer seats) is configured to support a single wafer thereon **during a pump down of the load lock**. (See Rivkin, col. 8, lines 34-66 which explains that only the pedestal **182** having a single wafer thereon is used "during a pump down of the load lock" **108** while the pedestal 184 is not used during pump down of the load lock.)

It would have been obvious for one of ordinary skill in the art, at the time of the invention to use the single-wafer load lock of **Rivkin**, in the process system of **Guo** to enable additional processing not typically provided in a load-lock, as is taught to be beneficial in **Rivkin** (Abstract and Summary of Invention).

Regarding claims 2, **Guo** shows process module **118** connected to the load chamber **113** (the first set of process modules) may be a pre-clean module (col. 4, line 7).

Regarding claims 3 and 4, **Guo** shows process module **121** connected to the load chamber 113 (the first set of process modules) may be a physical vapor deposition (PVD) or chemical vapor deposition (CVD) module (col. 4, lines 49-52).

Regarding claim 6, **Guo** shows process module **104** connected to the transfer chamber 101 (the second set of process modules) is a chemical vapor deposition (CVD) module (col. 4, lines 64-66).

Regarding claims 10, 11, and 21, **Guo** discloses that it is known for the intermediate process module **122** to be configured as either a cooling station or a pre-clean module (col. 1, 45-48; col. 4, line 47).

Regarding claim 12, **Guo** shows the intermediate process module **124** is configured as a PVD chamber.

Regarding claims 5, 7, 9, and 13, **Guo** does not specifically indicate that the second set of process modules (those on the transfer chamber **101**) include a pre-clean module (claim 5) or a PVD module (claim 7), or that the intermediate process module **122, 124** may be configured as a degas module (claim 9) or a CVD module (claim 13). Note however, that **Guo** teaches the benefits of configuring one of the intermediate chambers **122, 124** as a PVD module (col. 3, lines 43-50). Additionally, **Guo** teaches that the ordering of process modules is "illustrative" (col. 3, lines 60-63), and that cluster tools include a variety of ordered tools depending upon the process being performed (col. 1, lines 30-48), and also that metallization cluster tools include CVD, PVD, pre-clean and degas modules, among others (col. 2, lines 34-59 and through out the specification and figures). This suggests to one of ordinary skill in the art that the arrangement is a matter of design choice to best suit a given processing steps to be performed in a semiconductor wafer. Moreover, it has been held that mere rearrangement of parts is evidence of obviousness. *In re Kuhle*, 526 F.2d 553, 188 USPQ 7 (CCPA 1975) (the particular placement of a contact in a conductivity measuring device was held to be an obvious matter of design choice).

It would have been obvious for one of ordinary skill in the art, at the time of the invention to have a pre-clean module or PVD module in the second set of process modules and to have a degas and pre-clean modules as intermediate modules, in order to optimize the process

throughput for a given process, as taught by **Guo** and according to precedent. Moreover, Applicant indicates that virtually any arrangement of process modules is possible, thereby teaching away from the criticality of any specific arrangement in the processing system.

5. Claims **17** and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,251,759 B1 (**Guo** et al.) in view of US 5,281,320 (**Turner** et al.)

Regarding independent claims 1 and 17, **Guo** discloses a wafer processing system comprising:

a load lock **114** (Fig. 1);

a transport module having a load chamber **113** (called "buffer chamber" in Guo), a transfer chamber **101**, and a pass-through chamber **122** (additionally called "transition chambers" in Guo col. 4, line 19) located between the load chamber **113** and the transfer chamber **101**, the load chamber being coupled to the load lock **114**;

an intermediate process module **124** (called "transition chambers" in Guo col. 4, line 19) coupled to the load chamber and the transfer chamber (as further limited by instant claim 20);

a loader **130** configured to receive a plurality of wafers to be processed;

a robot **119** configured to transfer a wafer between the load lock **114** and the loader **130**, the robot **119** being exposed to atmosphere;

a first set of process modules **116, 118, 121** coupled to the load chamber **113**;

a second set of process modules **104, 106, 108, 110** coupled to the transfer chamber.

Note that the word "atmosphere" is taken to be that atmosphere within the buffer chamber.

Guo does not indicate if the load lock has "only one pedestal configured to support a single wafer thereon during a pump down of the load lock," as presently amended.

Turner teaches a single wafer load lock chamber **12** (Figs. 4-6) having only one pedestal **18** (called a "plate assembly" at col. 12, lines 20-37) configured to support a single wafer **15** thereon during a pump down of the load lock in a cluster tool (Figs. 1-2). Turner teaches that the benefit of load lock is that the volume is minimized to accommodate a single wafer in order to reduce the amount of pump down required for the load lock (col. 7, lines 12-16; col. 10, lines 24-39).

It would have been obvious for one of ordinary skill in the art, at the time of the invention to use a single-wafer load-lock having only one pedestal configured to support a single wafer thereon during a pump down of the load lock, as the load lock in **Guo**, in order to reduce the amount of pump down required for the load lock and thereby increase wafer processing throughput, as taught by **Turner**.

6. Claims **1**-7, 9-13 and 19, 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,251,759 B1 (**Guo** et al.) in view of US 5,281,320 (**Turner** et al.) and US 6,270,582 B1 (**Rivkin** et al.).

The prior art of **Guo** in view of **Turner**, as explained above, discloses each of the claimed features except for teaching that the single-wafer load-lock has an integral cooling unit for cooling the single wafer.

Rivkin teaches a single-wafer load lock (title) for a multi-chamber semiconductor wafer process module having water-cooled, single-wafer pedestal **136**, wherein the cooling unit is

integrally formed with the pedestal and the load lock chamber and uses water cooling to cool the single wafer --as further limited by instant claim 19 (Fig. 3; col. 6, lines 1-4, lines 37-47). **Rivkin**, like **Turner**, recognizes that the volume of the load lock should be minimized to increase throughput (col. 4, lines 25-29). **Rivkin** also teaches that preprocessing by pre-heating or cooling the single wafer increases the efficiency of processing throughput (col. 3, lines 18-36).

It would have been obvious for one of ordinary skill in the art, at the time of the invention to incorporate integral cooling into the load lock of **Turner** in order to perform preprocessing on the wafer and thereby increase processing throughput, as taught by **Rivkin**.

Regarding claims 2, **Guo** shows process module **118** connected to the load chamber 113 (the first set of process modules) may be a pre-clean module (col. 4, line 7).

Regarding claims 3 and 4, **Guo** shows process module **121** connected to the load chamber 113 (the first set of process modules) may be a physical vapor deposition (PVD) or chemical vapor deposition (CVD) module (col. 4, lines 49-52).

Regarding claim 6, **Guo** shows process module **104** connected to the transfer chamber 101 (the second set of process modules) is a chemical vapor deposition (CVD) module (col. 4, lines 64-66).

Regarding claims 10, 11, and 21, **Guo** discloses that it is known for the intermediate process module **122** to be configured as either a cooling station or a pre-clean module (col. 1, 45-48; col. 4, line 47).

Regarding claim 12, **Guo** shows the intermediate process module **124** is configured as a PVD chamber.

Regarding claims 5, 7, 9, and 13, **Guo** does not specifically indicate that the second set of process modules (those on the transfer chamber **101**) include a pre-clean module (claim 5) or a PVD module (claim 7), or that the intermediate process module **122**, **124** may be configured as a degas module (claim 9) or a CVD module (claim 13). Note however, that **Guo** teaches the benefits of configuring one of the intermediate chambers **122**, **124** as a PVD module (col. 3, lines 43-50). Additionally, **Guo** teaches that the ordering of process modules is "illustrative" (col. 3, lines 60-63), and that cluster tools include a variety of ordered tools depending upon the process being performed (col. 1, lines 30-48), and also that metallization cluster tools include CVD, PVD, pre-clean and degas modules, among others (col. 2, lines 34-59 and through out the specification and figures). This suggests to one of ordinary skill in the art that the arrangement is a matter of design choice to best suit a given processing steps to be performed in a semiconductor wafer. Moreover, it has been held that mere rearrangement of parts is evidence of obviousness. *In re Kuhle*, 526 F.2d 553, 188 USPQ 7 (CCPA 1975) (the particular placement of a contact in a conductivity measuring device was held to be an obvious matter of design choice).

It would have been obvious for one of ordinary skill in the art, at the time of the invention to have a pre-clean module or PVD module in the second set of process modules and to have a degas and pre-clean modules as intermediate modules, in order to optimize the process throughput for a given process, as taught by **Guo** and according to precedent. Moreover, Applicant indicates that virtually any arrangement of process modules is possible, thereby teaching away from the criticality of any specific arrangement in the processing system.

Double Patenting

7. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

8. Claims **1**-7, 9-13 and **17**, 19-21 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 2 of U.S. Patent No. 6,431,807 B1 (**Stevens** et al.) in view of US 6,251,759 B1 (**Guo** et al.).

Claims 1 and 2 of the Stevens patent claim a single-wafer load lock having only one pedestal configured to support a single wafer thereon, wherein the load-lock has an integral cooling unit to cool the single wafer and a transfer chamber and liquid cooling.

Guo teaches a wafer processing system having the remaining features of the claims, as explained above.

It would have been obvious for one of ordinary skill in the art, at the time of the invention to incorporate the cluster system of **Guo** into the single-wafer system of **Stevens**, in order to form the cluster tool having high throughput, as taught by **Guo**.

Response to Arguments

9. Applicant's arguments filed 18 December 2003 have been fully considered but they are not persuasive.

Applicant argues that the vacuum chuck is not a single wafer pedestal and that one of ordinary skill would not consider a vacuum chuck to be a single wafer pedestal. Examiner respectfully but emphatically disagrees. One of ordinary skill, would know very well that a vacuum is a single wafer pedestal, as the vacuum processing apparatus of the prior art is replete with vacuum chucks which are used specifically used to support a single wafer. As a matter of fact, a "vacuum chuck" is a specific example of a single wafer pedestal which employs a vacuum to hold the wafer in place during processing. Given the amendments to the claims, the point is moot.

In as much as the wafer is not suspended in space in **Turner**, **Turner** very clearly teaches a single wafer pedestal **18** used during the pump down. Accordingly, the art of **Guo** in view of **Turner** clearly teaches the instant invention as presently claimed in claim 17. It is noted that claim 17 has been broadened by no longer requiring the pedestal to have an integral cooling unit. Accordingly, **Rivkin** is no longer required to reject claims 17 and 20.

Applicant argues the **Guo** does not teach a loader. Examiner respectfully disagrees. The loader, **119, 130** is shown in **Guo**, as noted above in the rejection of claims. Accordingly, the argument is not found persuasive.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erik Kielin whose telephone number is 571-272-1693. The examiner can normally be reached on 9:00 - 19:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Erik Kielin
Primary Examiner
7 March 2004